Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to clarify Applicants disclosed and claimed invention.

Support for the amendments is found in the original claims and/or the Specification.

No new matter has been added.

For example, support for limitations in claims 1, 12, and 22 are found in Figures 3, 4A and 4B.

Additional support for new claim 22 is found in paragraph 0023 of the Specification:

"Inevitable polymer formation on the inner surfaces of the etch chamber 302 that subsequently peels off and falls down due to gravity does not land onto the wafer 320. This is because the wafer 320 is positioned over the plasma chamber 302, and not under the plasma chamber 302 as in the prior art.

That is, positioning of the wafer 320 over the chamber 302 prevents the excess polymer from landing onto the wafer 320. Thus, large and heavy polymer particles, which are not attracted to the wafer 320 because of their electrically neutral or lowly charged nature, fall harmlessly onto the dielectric window 308. This prevents defects from occurring on the semiconductor devices being fabricated on the wafer 320, increasing yield and decreasing cost to the semiconductor manufacturer."

Claim Rejections under 35 USC 103(a)

1. Claims 1, 3-5, 7-8, 11-12, 15-17, and 19 stand rejected under 35 USC 103(a) as being unpatentable over Ishi et al., (US 5,571,366) in view of Somekh et al. (US 5,643,366) or Brors et al.(EP 0276061).

Ishi et al. disclose a plasma processing apparatus whereby the plasma pressure or light emitted from the plasma is monitored in-situ and a voltage source for supplying a radiofrequency is controlled in response to the in-situ monitoring (see abstract).

In one embodiment a vertically moveable wafer support mechanism (see col 11, line 32-36; Figure 12, item 76) is disclosed to support a wafer held by an electrostatic chuck (item 12) in a face down position together with a vertically moveable pusher pin mechanism (item 77) embedded in the electrostatic

wafer chuck to remove the wafer from the electrostatic chuck following wafer processing. Ishi et al. does not disclose the structure of the vertically moveable support mechanism (item 76) other than what is shown in Figure 12. Figure 12 shows the wafer support (item 76) having a left and right fingers (arms) that support the wafer surface on the periphery (item W). Ishi et al. disclose that in the face down position, the wafer process surface can be protected from being contaminated by fine particles (col 11, lines 37-40).

Thus, the wafer support structure of Ishi et al. holds the wafer in an upside down position with an electrostatic wafer chuck and further **supported** from below by a **two fingered wafer lifter touching only the wafer periphery**.

Thus, Ishi et al. does not disclose the structure of Applicants claimed semiconductor wafer lifter including a bottom portion having a circular opening on which the semiconductor wafer periphery rests to expose only the semiconductor wafer processing surface face down during plasma processing.

Ishi et al. further does not disclose or suggest that an electrical bias is or can be supplied through a semiconductor wafer lifter. Rather in the apparatus of Ishi et al. the semiconductor wafer holder is taught only to be electrically biased through the electrostatic chuck.

Ishi et al. fail to disclose several aspects of Applicants disclosed and claimed invention. Moreover, and the wafer lifter of Ishi et al. operates by a different principal of operation

than the claimed structure of Applicants, i.e., touching the semiconductor process face **only at two points** on the wafer periphery with the two fingered wafer lifter, **while exposing side portions of the wafer.** The apparatus of Ishi et al., who do not disclose supplying an electrical bias as Applicants have claimed could not accomplish the purpose of Applicants disclosed and claimed invention.

Examiner argues that "as shown in Figure 12, the wafer lifter contacts portions of the apparatus that are applied with electrical bias and therefore, inherently, the wafer lifter will be supplied with an electrical bias."

Applicants respectfully point out that the wafer lifter is shown to contact only peripheral portions of the wafer process surface, which may be electrically insulated from the electrostatic chuck by an insulating layer commonly used in layered structures on a semiconductor processing wafer. There is no teaching in Ishi et al., that the wafer lifter is supplied with an electrical bias. Applicants respectfully reject any assertion of inherency by Examiner.

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Oelrich, 666 F.2d 578, 581-582, 212 USPQ 323, 326 (CCPA 1981).*

Somekh et al., on the other hand discloses a "C" shaped wafer support (wafer lifter) with a **three fingered contact**

surface to raise a semiconductor wafer to contact a susceptor (wafer chuck) (see abstract, col 2, lines 6-18;). The wafer lifter (wafer support assembly) is **then lowered and moved out of the path of the susceptor** (col 2, lines 26-30) which is lowered **for plasma processing**. The purpose of the "C" shaped wafer support is to allow a susceptor arm to move the susceptor holding the wafer downward into a plasma processing position after the wafer support is removed from the wafer (col 3, lines 1-8).

Brors et al. disclose a plasma chamber for CVD deposition including a manipulator arm and blade (wafer lifter) that transfers a wafer from a cassette in a loading chamber to underneath a wafer chuck located at a top portion of the plasma chamber by rotating horizontally 90 degrees. A **3-arm lifting mechanism** on the blade, each arm having ceramic fingers then lifts the wafer to contact the chuck, similar to Somekh et al.:

"The manipulator arm 68 is rotated by a motor through a 90 DEG angle. The loadlock 64 is opened and the manipulator arm 68 extends carrying the blade 70 with wafer 46 into the center of the deposition chamber 16. **Three lifting arms** 72 **each having a ceramic finger** 74 approximately one-eighth inch in diameter attached to support 71, lift the wafer 46 off the blade and contact the back side of the wafer 46, face down, with the chuck 76.A larger number of ceramic fingers can be used to avoid the necessity of prealigning the wafer to orient the flat, however, **typically 3 fingers are used with prealignment** of the wafers in the cassette."

Neither Somekh et al. or Brors et al. teach a wafer lifter having the structure and operation of Applicants disclosed and

claimed invention including holding the wafer in a face down processing position **during plasma processing** at a top of the plasma chamber with an electrical bias supplied to the **semiconductor wafer and the semiconductor wafer lifter.**

Thus, the structure of the wafer support (lifter) of Somekh et al. or Brors et al. is different from both Ishi et al. and Applicants disclosed and claimed invention. The wafer lifter of Somekh et al. or Brors et al. does not hold the wafer at a top of the plasma chamber **during plasma processing,** but rather raises the wafer to contact a susceptor (wafer chuck), which hold the wafer during processing while the wafer lifter **is move out of the way of the plasma process.** Thus, the wafer lifter of Somekh et al. or Brors et al. works by a different principal of operation compared to Ishi et al. as well as Applicants disclosed and claimed invention, and directly **teaches away** from Applicants disclosed and claimed invention.

Thus, there is no apparent motive for combining the teachings of Ishi et al. with Somekh et al. or Brors et al. For example, holding the wafer at a top portion of the plasma chamber during processing (as shown in Ishi et al.) with the wafer lifter of Somekh et al. or Brors et al. would destroy the principal of operation of the wafer lifter of Somekh et al. or Brors et al., interfering with movement of the susceptor as taught by susceptor as well as interfering with a plasma process such as etching or CVD deposition. Conversely, removing the wafer lifter prior to plasma processing or moving the susceptor downward to avoid the wafer lifter for processing as taught in the operation and structure of the apparatus of Somekh et al. or Brors et al. would

destroy and make unworkable the principal of operation of the apparatus of Ishi et al., since the wafer lifter of Ishi et al. supports the wafer in a face down position during processing.

Nevertheless, even assuming *arguendo* a proper motive for combining Ishi et al. and Somekh et al. or Brors et al., such combination does not produce Applicants disclosed and claimed invention. None of the references, alone or in combination, discloses the structure and operation of Applicants wafer lifter. Moreover none of Ishi et al., Somekh et al. or Brors et al., alone or in combination suggest, disclose or teach supplying an electrical bias to the wafer lifter during processing.

The **two fingered structure** of Ishi et al. and the **three fingered structures** of Somekh et al. or Brors et al., could not accomplish the principal of operation including supplying a bias to the wafer lifter during plasma processing as claimed and disclosed by Applicants.

Moreover, the combined teachings of Ishi et al., Somekh et al. or Brors et al. do not show the following elements of Applicants disclosed and claimed invention:

"wherein the semiconductor wafer periphery rests on an inner top surface of the bottom portion defining the circular opening to expose only the semiconductor wafer processing surface face down during plasma processing."

The combined teachings of Ishi et al., Somekh et al. and/or Brors et al. are clearly insufficient to make out a *prima facie*

case of obviousness with respect to Applicants disclosed and claimed invention.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

"A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler,* 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc.,*

721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).

Examiner argues that regardless of the differences in the structure of Applicants disclosed and claimed invention and the combined teachings of Ishi et al. and Somekh et al. or Brors et al., that "a *prima face* case of obviousness still exists because no unexpected results have been shown". Applicants respectfully suggest Examiner is mistaken in suggesting that Applicants have a required showing of unexpected results, when a *prima facie* case of obviousness with respect to Applicants disclosed and claimed invention has not yet been made out.

The "unexpected results" analysis applies to processes involving claimed ranges (see MPEP 2131.03). Moreover, "unexpected results" are to be considered by the Examiner upon submission by the Applicants in order to overcome a *prima facie* case of obviousness where patentability depends on claimed overlapping ranges. A *prima facie* case of obviousness has not yet been made out by Examiner since Applicants disclosed and claimed invention has not been shown in the prior art by the cited references individually or in combination.

Examiner argues that the fact that Somekh et al. or Brors et al. do not show the wafer lifter holding the wafer in place during plasma processing, is merely a recitation of intended use. However, as pointed out above, the apparatus of Somekh et al. or Brors et al. **would not work as intended** if the wafer were supported during plasma processing, i.e., **interfering with the**

plasma processing operation, thereby making the apparatus unsuitable for its intended use (i.e. **incapable of performing the intended use**). Moreover, the "intended use" argument to establish a prima facie case of obviousness, first requires a showing in the prior art of Applicants claimed structure, which Examiner has not accomplished.

2. Claim 9 stands rejected under 35 USC 103(a) as being unpatentable over Ishi et al., (US 5,571,366) in view of Somekh et al. (US 5,643,366) or Brors et al. (EP 0276061), as applied above, and further in view of Uchida (US 5,804,027) or Ishi et al. (US 5,795,429).

Applicants reiterate the comments made above with respect to Ishi et al., Somekh et al. or Brors et al.

In addition, even assuming arguendo, proper motivation for combination, the combination of the teachings of Ishi et al., with Somekh et al. or Brors et al., and further in view of Uchida or Ishi et al. '429, does not produce Applicants disclosed and claimed invention and does not help Examiner in making out a *prima facie* case of obviousness.

Applicants point out that "we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v.*

Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

3. Claims 10 and 18 stand rejected under 35 USC 103(a) as being unpatentable over Ishi et al., (US 5,571,366) in view of Somekh et al. (US 5, 643, 366) or Brors et al. EP 0276061, as applied above, and further in view of Admitted Prior Art.

Applicants reiterate the comments made above with respect to Ishi et al., Somekh et al. or Brors et al.

Applicants further respectfully point out that Examiner is erroneously looking to Applicants disclosure **for a suggestion to combine the teachings of references**, i.e., as a roadmap to recreate Applicants disclosed and claimed invention, which Applicants respectfully point out is impermissible.

Nevertheless, in Applicants discussion of the prior art, Applicants merely disclose problems with a plasma processing chamber where a wafer is held in a face-up position during plasma processing. Thus, even assuming *arguendo*, proper motivation for combination, the combination of Ishi et al. with Somekh et al. or Brors et al., and further in view of Applicants alleged admitted prior art, does not produce Applicants disclosed and claimed invention and does not further help Examiner in making out a

prima facie case of obviousness.

"The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and **not based on applicant's disclosure.**" *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

4. Claims 1, 3, 5, 7-8, 10-12, and 15-19 stand rejected under 35 USC 103(a) as being unpatentable over Admitted Prior Art in view of Ishi et al., (US 5,571,366), and Somekh et al. (US 5, 643, 366) or Brors et al. (EP 0276061).

Applicants reiterate the comments made above with respect to Applicants alleged admitted prior art, Ishi et al., and Somekh et al. or Brors et al.

In addition, even assuming *arguendo*, proper motivation for combination, the combination of Applicants alleged admitted prior with and Ishi et al., Somekh et al. or Brors et al., does not produce Applicants disclosed and claimed invention and does not further help Examiner in making out a *prima facie* case of obviousness.

Applicants again point out that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and **not based on**

applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

5. Claim 9 stands rejected under 35 USC 103(a) as being unpatentable over Admitted prior art in view of Ishi et al. (US 5,571,366), and Somekh et al. (US 5, 643, 366) or Brors et al. EP 0276061, as applied above, and further in view of Uchida (US 5,804,027) or Ishi et al. (US 5,795,429).

Applicants reiterate the comments made above with respect to Applicants alleged admitted prior art, Ishi et al., and Somekh et al. or Brors et al.

In addition, even assuming *arguendo*, proper motivation for combination, the combination of Applicants alleged admitted prior with and Ishi et al., and Somekh et al. or Brors et al., and further in view of Uchida or Ishi et al. '429, does not produce Applicants disclosed and claimed invention and does not help Examiner in making out *a prima facie* case of obviousness.

Applicants have amended their claims to clarify their invention. Based on the foregoing, the Applicants respectfully submit that the claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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